A Novel Design of Current Mode Multiplier/Divider Circuit Using Translinear Principle

M. Mohankumar¹, R. Gowrimanohari²

¹Assistant Professor, mail2mohanphd@gmail.com, Sri Eshwar College of Engineering, India
²Pg Student, gowri.mano3@gmail.com, Sri Eshwar College of Engineering, India

Abstract

In analog signal processing, current is used as input variables. In this design current mode multiplier/divider circuits is implemented using translinear principle. Thus implementing the circuit with translinear concept has small linearity errors. In addition, high linearity is achieved because high accuracy current mirror is adopted between the squarer circuits and the output current is insensitive to the temperature. The proposed multiplier/divider circuit is designed for implementing in 0.18-μm CMOS technology, with a low-voltage operation (a supply voltage of 1V) excepting with the power consumption of 65μW while their frequency bandwidth is 44MHz.

Index Terms- Analog signal processing, current-mode operation, multiplier, and translinear.

1. Introduction

Signal processing circuits find a large number of applications in many domains such as telecommunications, medical equipment, hearing devices, and disk drives, the preference for an analog approach of signal processing systems being mainly motivated by their low-power operation and high speed that allows a real-time signal processing. Analog signal processing represents the signals as physical quantities like e.g. charge, current, voltage or frequency. These signals are continuous in value and continuous in time. Analog signal processing is most effective when precision is not the major criteria and when massive parallel collective processing of large number of signals that are continuous in time and amplitude is required [11].

Multiplication and division of analog signals are difficult operations in analog signal processing. Analog multipliers and dividers are used in communication circuits as well as in neural networks and fuzzy logic applications. Phase detector, adaptive filter, function generators, frequency doubling and amplitude modulation is some applications of analog multipliers in communications industry. Voltage gain amplifier, signal squarer, RMS signal estimator and weight-input multiplication in neural networks are some application in signal processing. Analog multipliers as part of automatic gain control circuits used in AM radio receivers and radar system. Low supply voltages, low bias currents, low effective threshold voltages of MOS transistors are some methods to reduce power consumption in multiplier and divider architectures.

In order to improve the frequency response of the computational structures and to increase their −3 dB bandwidth, many analog signal processing functions can be achieved by exploiting the squaring characteristic of MOS transistors biased in saturation. In [6], multiplier structures were presented with single-ended input voltages, the linearization of their characteristics being obtained using proper squaring relations between the input potentials. In order to implement the multiplication of two differential-input voltages, in [5] multiplier circuits were described based on mathematical principles, similar to the methods used for multipliers with single input voltages. The biasing of the multiplier differential core at a current equal to the sum of a constant component and a current proportional to...
the square of the differential input voltage was presented in [7] and [8] and allows us to obtain a linear behavior of the implemented multiplier circuits. In another class of multipliers [7], currents are used as input variables. In this case, the designed circuits present the advantage of an independence of the circuit performances on technological errors. These circuits can implement, based on the same configuration, both multiplying, and dividing functions. Multiplier structures were also reported [7]–[9] with increased linearity, designed using different mathematical principles.

2. Translinear Principle

Translinear circuit principle which was originally formulated for loops of bipolar transistors is generalized and the MOS translinear (MTL) principle is derived by Seevinck [12]. MTL circuits are designed by applying MTL principle and used in synthesizing many nonlinear signal processing functions. Square-root circuit and squarer/divider circuit are two important structures of the MTL circuits. A multiplier/divider circuit can be obtained by using both square-root and squarer/divider circuit as in Figure 1. A translinear circuit should have inputs and outputs in the form of currents and no voltages other than the junction voltages are involved. Initial translinear (TL) circuits used exponential current-voltage characteristics of bipolar transistors. MOS translinear (MTL) circuits are designed using exponential I-V characteristics in sub threshold region. But dynamic range and speed of operation of such circuits are limited due to MOS transistors operating in weak inversion. The widely used MTL circuits are based on linear relationship between transconductance and voltage [12]. Compared to BTL circuits MTL circuits have less current range, bounded at low end by weak inversion and at high end by mobility reduction. But MTL circuits have better matching properties and zero gate leakage current. In MTL circuits all transistors operate in saturation region and generalized TL equation for loop connected MOS transistors is given by

$$\sum_{cw} \sqrt{I_d/W/L} = \sum_{ccw} \sqrt{I_d/W/L}$$  \hspace{1cm} (1)

![Image of Voltage-translinear loop based stacked topology](image)

Figure.1 Voltage-translinear loop based stacked topology

The stacked VTL circuit gives geometric mean of input currents. Assuming identical transistors, W/L ratios of all transistors becomes same and equation (1) reduces to

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4}$$  \hspace{1cm} (2)

Hence, several nonlinear current-mode functions can be implemented by properly injecting such currents. For instance, if we force

$$I_3 = I_4 = \frac{I_1 + I_2 + 2I_5}{4}$$  \hspace{1cm} (3)
Being \( I_5 \) a certain current, after squaring both sides in (3) and rearranging, currents \( I_1, I_2 \) and \( I_5 \) become related by

\[
I_5 = \sqrt{I_1 I_2}
\]  
(4)

Therefore, a geometric-mean circuit is obtained if \( I_1 \) and \( I_2 \) are the input currents and the output current is a copy of \( I_5 \).

![Figure 2. Principle of the multiplier/divider circuit](image)

### 3. Low-Voltage Squarer Circuit

![Figure 3. The low-voltage squarer circuit](image)

The diode-connected MOSFET of the current mirror precludes very low voltage operation due to the stacking of two diode-connected transistors. Equation (4) can be alternatively implemented using the novel topology of Fig.3. Now a circuit is formed by transistors \( M_1 \) and \( M_{F1} \), sets the proper reference dc voltage at the loop nodes. The main advantage of this structure is that the source of \( M_1 \) is a very low impedance node, so that voltage at this node is kept essentially constant regardless of the input and output current.
The minimum supply voltage is limited by the path formed by $I_b$, $M_1$ and $M_{F1}$ so the minimum supply voltage is

$$V_{DD}^{\text{min}} = V_{th} + 3V_{DS_{sat}} = 0.55 = 3 \times 0.1 = 0.85V$$

(5)

where $V_{G_{SF}}$ is gate-source voltage of $M_{F2}$, $V_{DS_{sat}}$ is the minimum voltage drop in current source $I_b$ and can be as small as 0.1V in 0.18μm where $V_{th}=0.55$ V for NMOS.

Thus the selected $V_{DD}=1V$ in order to have an appreciable voltage swing.

4. Current-Mode Multiplier /Divider Circuit

The multiplication of two signals is one of the most important operations in analog signal processing. Especially, the short-channel effects become more important in MOS transistors at channel lengths of about 1μm or less and require modifications to the MOS models as well as the circuits that are designed using these MOS transistors. Due to the second order effects small sized MOS transistors don’t operate properly and therefore errors may occur in the output current function of the current-mode circuits employing these transistors.

![Multiplier/divider circuit](image)

Figure 4. Multiplier/divider circuit

5. Simulation Results

To verify the proposed circuit, SPICE simulation were performed and the current multiplier in Fig.4 was laid out in standard 0.18μm CMOS technology. The power supply voltage is 1.2V. The $I_{OUT}(I_1)$ simulation for the multiplier/divider circuit proposed in Fig. 5. The $I_{OUT}(I_2)$ simulation for the multiplier/divider circuit proposed in
Fig. 6. The simulation output of ac sweep analysis for the multiplier/divider circuit proposed in Fig. 7. The simulation output of linearity error for the multiplier/divider circuit proposed in Fig. 8.

**Figure 5.** Simulation output for multiplier circuit $I_{out}$ ($I_1$)

**Figure 6.** Simulation output for multiplier circuit $I_{out}$ ($I_2$)
Figure 7. Simulation output of ac sweep analysis

Figure 8. Simulation output for linearity error

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<thead>
<tr>
<th>Parameters</th>
<th>Ref paper 1</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology[μm]</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>Supply Voltage[V]</td>
<td>1.2</td>
<td>1</td>
</tr>
<tr>
<td>Power Consumption[μW]</td>
<td>75</td>
<td>65</td>
</tr>
<tr>
<td>Linearity Error[%)</td>
<td>0.9</td>
<td>0.66</td>
</tr>
<tr>
<td>Bandwidth[MHz]</td>
<td>59.7</td>
<td>44</td>
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</tbody>
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6. Conclusion

A current mode multiplier/divider circuit based on properties of a translinear loop is described. The proposed structure has extremely low linearity error (0.66%). The minimum value for the supply voltage of 1V was obtained for implementing the proposed computational structure in 0.18-μm CMOS technology. It is possible to also implement the proposed circuit in processes of 40 or 28 nm, having much lower value of the threshold voltage and, in consequence, allowing a much smaller value of the minimal supply voltage (even less than 1 V). The circuit bandwidth is 44 MHz, while their power consumption is extremely low.
References


